AMENDMENTS TO THE CLAIMS

1-33. (Canceled)

34. (New) A signaling circuit for encoding presence detect data comprising:

a first signal encoding portion for encoding first information, said first information being disposed in a hard-wired circuit of a semiconductor memory device, said hard-wired circuit formed during manufacturing of said semiconductor memory device; and

a second signal encoding portion for encoding second information said second information being disposed in a programmable circuit of said semiconductor memory device, said programmable circuit programmed subsequent to manufacturing of said semiconductor memory device.

35. (New) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a storage capacity of said semiconductor memory device.

36. (New) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a data bus width of said semiconductor memory device.

37. (New) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a data access speed of said semiconductor memory device.

38. (New) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a column address strobe latency of said semiconductor memory device.

39. (New) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to a data refresh rate of said semiconductor memory device.

40. (New) A signaling circuit as defined in claim 34 wherein said presence detect data comprises:

data relating to an interface voltage of said semiconductor memory device.

41. (New) A signaling circuit as defined in claim 34 wherein said first signal portion and said second signal portion comprise first and second serial data signals respectively, said first and second serial data signals being adapted to be transmitted over a single data line.

42. (New) A signaling circuit as defined in claim 34 wherein said programmable circuit comprises a fuse device.

43. (New) A signaling circuit as defined in claim 34 wherein said programmable circuit comprises an antifuse device.

44. (New) A signaling circuit as defined in claim 34 wherein said programmable circuit comprises a transistor-based device.

45. (New) A method of forming a semiconductor memory device comprising:

forming a presence detect data circuit on a common substrate with a memory storage circuit, said presence detect data circuit including a plurality of data bit devices;

depositing a conductive mask above said substrate;

fixing a data-storage state of a first subset of data bit devices with said conductive mask, said first subset of data bit devices including one or more of said plurality of data bit devices; and

programming a second subset of data bit devices, said second subset of data bit devices including one or more of said plurality of data bit devices.

46. (New) A method of forming a semiconductor memory device as defined in claim 45 wherein said fixing a data-storage state comprises:

short-circuiting said first subset of data bit devices.

47. (New) A method of forming a semiconductor memory device as defined in claim 45 wherein said fixing a data-storage state comprises:

open-circuiting said first subset of data bit devices.

48. (New) A method of forming a semiconductor memory device as defined in claim 45 wherein said programming a second subset of data bit devices comprises:

laser fusing said second subset of data bit devices.

49. (New) A method of forming a semiconductor memory device as defined in claim 45 wherein said programming a second subset of data bit devices comprises:

electrically fusing said second subset of data bit devices.

50. (New) A method of forming a semiconductor memory device as defined in claim 45 wherein said plurality of data bit devices comprises a plurality of flash transistors.

51. (New) A method of forming a semiconductor memory device as defined in claim 45 further comprising:

forming a multiplexer circuit on said substrate, said multiplexer circuit including a presence detect data input port and a control input port; and

coupling one or more of said plurality of data bit devices to said presence detect data input port.

52. (New) A method of forming a semiconductor memory device as defined in claim 51 further comprising:

forming a counter circuit on said substrate;

coupling an output port of said counter circuit to said control input port of said multiplexer circuit; and

coupling an input port of said counter circuit to a toggle control signal input of said semiconductor memory device.

53. (New) A method of operating a memory integrated circuit comprising:

receiving a first signal at a memory controller from said memory integrated circuit, said first signal encoding first information hardwired into said memory integrated circuit during manufacturing of said memory integrated circuit; and

receiving a second signal at a memory controller from said memory integrated circuit, said second signal encoding second information programmed into said memory integrated circuit subsequent to manufacturing of said memory integrated circuit.

54. (New) A method of operating a memory integrated circuit as defined in claim 53 further comprising:

receiving a control signal at said memory integrated circuit from said memory controller, said control signal being related to at least one of said first signal and said second signal.

55. (New) A method of operating a memory integrated circuit is defined in claim 53 further comprising:

receiving an address signal at said memory integrated circuit from said memory controller, said address signal having a format related to at least one of said first signal and said second signal.

56. (New) A method of operating a memory integrated circuit as defined in claim 53 further comprising:

recognizing an identity of said memory integrated circuit at said memory controller based on said first and second signals.

57. (New) A method of operating a memory integrated circuit as defined in claim 53 wherein said first and second information comprises presence detect data.

58. (New) A method of forming a semiconductor memory device comprising:

forming a presence detect data circuit on a common substrate with a memory storage circuit, said presence detect data circuit including a plurality of data bit devices;

fixing a data-storage state of a first subset of said plurality of data bit devices during a first time interval;

processing said substrate during a second time interval, said second time interval being subsequent to said first time interval; and

programming a second subset of said plurality of data bit devices during a third time interval, said third time interval being subsequent to said second time interval.

59. (New) A method of forming a semiconductor memory device as defined in claim 58 wherein said processing said substrate during a second time interval comprises encapsulating said substrate during said second time interval.